K-1008-6 INTEGRATED VISIBLE MEMORY

FOR PET AND CBM COMPUTERS

8K BYTE MEMORY

320 WIDE BY 200 HIGH DOT MATRIX DISPLAY

LIGHT PEN REGISTER

ROM SOCKET EXPANSION

KIM BUS INTERFACE

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K-1008-6 UNPACKING AND INSTALLATION

The K-1008-6 Integrated Visible Memory for the PET is a carefully engineered, manufactured, and tested product that should operate perfectly when handled and installed according to the following instructions. Note that the board is shipped in a black conductive plastic bag. Since MOS integrated circuits are used, damage from static discharge is possible. It is helpful to reduce static by working in an area with concrete floors and a reasonable humidity level. If this is impossible, at least avoid wearing rubber soled shoes and move slowly in the work area. When unpacking or handling the board, touch the screw sticking up in the middle of the heatsink first and release it last. Note that the preceeding comments apply equally to the user's computer board which of course contains MOS IC's also.

ADDRESS AND FUNCTION SELECT JUMPERS

Due to the variety of PET configurations, the K-1008-6 Integrated Visible Memory has a number of address and function select jumpers. However the board is shipped with a "standard" jumper configuration installed which should be suitable for a large number of customers. This standard configuration is described below:

1. Type of PET - new style with 32K of original equipment memory

2. Visible memory low address - 9000-9FFF

3. Visible memory high address - A000-AFFF

4. ROM socket addresses - socket 1 9000-9FFF
   socket 2 A000-AFFF
   socket 3 B000-BFFF
   socket 4 9000-9FFF
   socket 5 A000-AFFF

5. External KIM bus addresses - PET addresses 2000-7FFF translate to KIM addresses 0000-5FFF. PET addresses A000-BFFF translate to KIM addresses 6000-7FFF.

6. Device enables - Visible Memory low - disabled
   Visible Memory high - disabled
   ROM socket 1 - enabled
   ROM socket 2 - enabled
   ROM socket 3 - enabled
   ROM socket 4 - disabled
   ROM socket 5 - disabled
   External KIM bus - disabled

7. Light pen registers - disabled (Note that the standard board comes without the light pen register IC's. See the light pen section for further discussion.)

8. Video iming - set for best video overlay on new style PET's.

Thus, when the board is installed and powered up, everything on the board except the first three ROM sockets is disabled. If at all possible, installation and initial test of the board should be with this standard configuration. Following testing of the board, the jumper configuration may be changed to suit individual needs by referring to the section entitled Jumper Options.

INSTALLATION INTO OLD STYLE PET'S

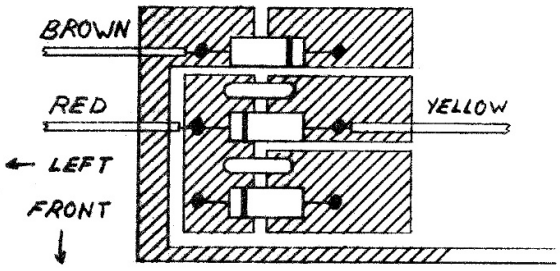
In order to install the K-1008-6 into an old-style PET the customer must obtain a K-1007-2 connector board. This board plugs onto the old-style PET memory expansion connector and provides a 60 wire ribbon cable connector that mates with the K-1008-6 ribbon cable. It also connects to the PET's video output and its monitor video input. Follow the instructions below to install and test the two boards:

1. Remove the 4 screws on the underside of the PET cover to allow the top half of the system to be tilted up.

2. Inspect for shipping damage to the boards and the ribbon cable. also inspect the board bottoms for shorts caused by bent-over component leads or embedded metal shavings.

3. Plug the small printed circuit board marked K-1007-2 onto the PET memory expansion fingers. The board should be positioned so that the ribbon cable connector and other assorted wires and connectors are facing upwards. At this time the large K-1008-6 board and its ribbon cable should not be connected to the K-1007-2.

4. Take the 3 separate wires (brown, red, and yellow) and solder them to the indicated large power diodes on the PET main logic board as shown to the right:

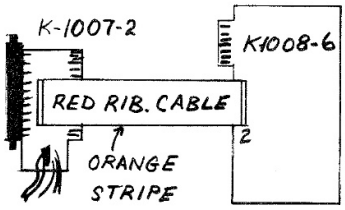


5. Leave the small white connector with three twisted-pair wires disconnected until later.

6. Turn the PET power on. Operation should be completely normal and not impaired in any way. The interface must pass this test before continuing with the next step. If the normal READY message does not appear, immediately turn power off and check the installation. Check to see if the small board is plugged onto the PET memory expansion port straight and is fully seated. Recheck the three power wires to be sure they were installed properly and try again. If normal PET operation cannot be obtained, turn power off and carefully unplug the K-1007-2 from the memory expansion connector and try again. If still no luck, remove the power wires and verify that normal PET operation is restored. If no cause for the malfunction can be found, return the K-1007-2 to the factory for warrenty repair or replacement.

7. Turn the PET power OFF!

8. Lay the K-1008-6 logic board flat on a non-metallic surface with the component side up and plug the large red ribbon cable from it into the K-1007-2 as illustrated below:



9. Turn the PET power on. Operation should again be completely normal. If it is not, turn the power off and check that both ribbon cable connectors engage all 60 pins (i.e. not skewed one position left or right). If it becomes necessary to unplug the ribbon cable, carefully pry off the connector with a screwdriver.

10. Turn the PET power OFF and remove the 7 position (6 wires and 1 polarizing pin) video connector which connects the PET main logic board to the display monitor. NEVER OPERATE THE PET WITH THE MONITOR DISCONNECTED. The ungrounded monitor will develop a high potential on its ground and destroy circuits when it is later plugged back into the PET or K-1007-2.

11. Plug the white connector from the K-1007-2 board onto the pins which are now exposed because the video cable was removed. It should be plugged on such that the three twisted-pair wires exit the connector toward the right.

12. Plug the PET video cable connector removed in step 9 onto the black connector on the K-1007-2 board. Polarizing pins in the connectors should prevent incorrect installation in steps 11 and 12.

13. Turn the PET on again. Operation should still be normal. If the monitor screen should fail to light up, immediately turn power off and check installation of the two video cables.

14. Type the following command into BASIC: POKE 49151,2 and then a carriage return. The screen should display a stable but semi-random dot pattern. If the screen goes blank after switching, immediately turn power off and check installation of the video cables and the K-1008-6.

15. Type the following command into BASIC: POKE 49151,3 and then a carriage return. The screen should now display the semi-random pattern and normal PET video overlayed (it will probably be impossible to actually read the PET screen but its presence should be obvious. The leftmost column of PET video dots should be 8 dots to the left of the leftmost column of Visible Memory dots. (The previous assumes the standard jumper configuration. There is a jumper that can be moved to make the dots line up more closely on the old PET's; see the section entitled Jumper Options).

16. Type the following command into BASIC: POKE 49150,1 and then a carrige return. The normal PET display should return.

17. Type the following command into BASIC: POKE 49151,3 and then a carriage return. The screen should again show VM and PET video overlayed. Next, locate the 7-pin black connector (2 of the pins have been cut off) at the rear of the K-1008-6 board. Momentarily short the two pins closest to the trimpot with a screwdriver. The standard PET display should return. This is the user RESET for the K-1008-6 and is used to restore PET video and default device enables after a program malfunction. The user may attach a remote pushbutton switch to this connector if desired.

18. Type in the diagnostic program listed in the back of this manual. It verifies that the Visible Memory portion of the board functions correctly as a memory.

19. Type in the short demonstration program listed in the back of this manual. It will switch to Visible Memory, plot a sine wave, wait for about 10 seconds, and then switch back to PET video.

20. This completes the installation and initial testing of the K-1007-2 and K-1008-6 in an old style PET. See the Operation section for detailed operation instructions. Also see the Jumper Options section for information on configuring the Integrated Visible Memory for maximum benefit on an old style PET.

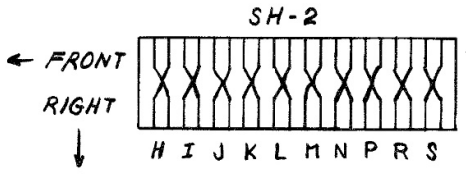
INSTALLATION INTO NEW STYLE PET'S OR CBM'S

Before starting the installation procedure, remove the 4 screws on the underside of the PET cover to allow the top half of the system to be tilted up. Look inside the PET on the right hand side of the PET's printed circuit board about 2/3 of the way toward the rear. There should be two sets of two parallel rows of 25 small square posts sticking up. If edge fingers are instead seen, it is an old style PET and the previous installation procedure must be used. Measure the gap between the two sets of pins. If it is .2 inches, the K-1007-3 connector board should be used with the K-1008-6. If it is .4 inches, a K-1007-4 connector board should be used.

PET JUMPER SETTING

NOTE: If you do not wish to modify the PET's internal jumpers, read the System Configuration section before installing the board. There may be an acceptable configuration listed that will not require the PET's jumpers to be changed.

Just to the left of the rearmost set of pins should be a set of jumpers that looks somewhat like an integrated circuit. The setting of these jumpers controls various buffers inside the PET. If they are not properly set, the PET will not be able to read from the K-1008-6 and the graphic software may not work properly. The jumper IC is a 20 pin device with thin metal links connecting pin 1 to 20, 2 to 19, ..., 10 to 11. When a link is intact or bridged with solder the jumper is said to be closed. When a link is cut with a knife it is said to be open. A small, sharp knife is required to cut the links. By far the best type to use is called an X-ACTO knife with a type 16 blade installed. Hobby shops usually have these and they are inexpensive. When using the knife, shield your eyes as it is possible to break the blade while severing a link. If the link to be severed had previously been bridged with solder, use of solder wick is recommended to remove the solder. Each of the 10 links is identified by a letter as shown in the drawing below:



Normally the jumpers are set only once. If frequent change is anticipated, one may cut all of the links and then straddle a 10 position dipswitch over the jumper block and solder it in place. This allows rapid change when desired.

Basically there are three possibilities according to the built-in memory capacity of the PET. The tables below show what to do for each possibility:

8K	16K	32K
Links open: H I K N R Links closed: J L M P S Visible Memory addressed at 2000 and 3000. PET ROM sockets are functional.	Links open: K L H N R Links closed: I J M P S Visible Memory addressed at 4000 and 5000. PET ROM sockets are functional.	Links open: K L M P R Links closed: H I J N S Visible Memory addressed at 9000 and A000. The 3 empty PET ROM sockets are disabled (sockets on K-1008-6 must be used)

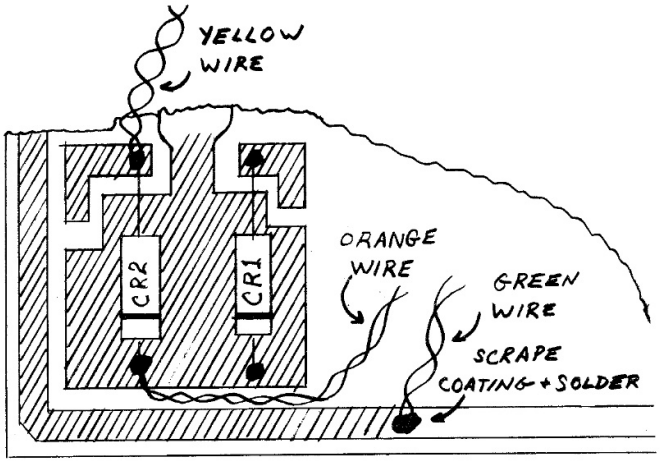
STEP-BY-STEP PROCEDURE

1. After setting the PET jumpers (if changed), turn on the PET and verify that normal operation has not been impaired. If it does not function normally, turn the power off and double-check the jumper settings, both closed and open.

2. Inspect the two boards for any signs of shipping damage. Also inspect the board bottoms for shorts caused by bent over component leads or embedded metal shavings.

2. Plug the small printed circuit board marked K-1007-3 onto the PET memory expansion posts. The board should be positioned so that the red ribbon cable and other assorted wires and connectors are facing toward the left of the PET. Be careful to line up the two black sockets of the K-1007-3 with the pins on the PET. A one position offset error is easy to make and would prevent proper operation. When plugging the connector board onto the PET, use a stack of index cards between the PET printed circuit board and bottom of the PET cabinet to prevent bending of the PET printed circuit board due to installation pressure. If it becomes necessary to separate the two boards later, very carefully rock the K-1007-3 and ease it off straight. Excessive force will result in a sudden release of the K-1007-3 and certain bending of the PET's connector pins. At this time the large K-1008-6 board should not be connected to the ribbon cable.

3. The K-1007-3 board should have been received with the power cable already plugged in. If not, the power cable may be identified as having twisted orange, yellow, and green wires but no white wires. Plug it onto the black connector on the K-1007-3 that has all 7 pins present. It may be plugged in either direction but it is easiest with the wires pointing upward. The other end of the power cable must be soldered to the rectifier diodes at the front left of the PET printed circuit board as illustrated to the right:



4. Leave the small white connector with three twisted-pair wires disconnected until later.

5. Turn the PET power on. Operation should be completely normal and not impaired in any way. The interface must pass this test before continuing with the next step. If the normal READY message does not appear, immediately turn power off and check the installation. Check to see if the K-1007-3 is plugged onto the PET memory expansion port straight and is fully seated. Recheck the three power wires to be sure they were installed properly and try again. If normal PET operation cannot be obtained, carefully unplug the K-1007-3 from the memory expansion connector and try again. If still no luck, remove the power wires and verify that normal PET operation is restored. Then carefully inspect the K-1007-3 board for shorts caused by bent over component leads or embedded metal shavings. If no cause for the malfunction can be found, return the K-1007-3 to the factory for warrenty repair or replacement.

6. Turn the PET power OFF!

17. Type in the diagnostic program listed in the back of this manual. It verifies that the Visible Memory portion of the board functions correctly as a memory. Be sure to alter the Visible Memory starting address in the program if the VM address jumpers were changed on the K-1008-6 board.

18. Type in the short demonstration program listed in the back of this manual. It will switch to Visible Memory, plot a sine wave, wait for about 10 seconds, and then switch back to PET video. Be sure to alter the Visible Memory starting address if the VM address jumpers were changed on the K-1008-6 board.

19. This completes the installation and initial testing of the K-1007-3 and K-1008-6 in a new style PET. See the Operation section for detailed operation instructions. Also see the Jumper Options section for information on configuring the Integrated Visible Memory for maximum benefit on any of the several types of new style PET's.

FINAL INSTALLATION

Although the K-1008-6 will operate perfectly OK outside the PET, most customers will prefer to mount it inside the PET case for protection. Special mounting brackets are available to properly support the board inside either a new PET or an old PET. Order number K-1005-5 ($10.00 per set) for new style PET's or number K-1005-6 ($15.00 per set) for old style PET's.

If you attempt to mount the board without the brackets, be certain that none of the printed wiring traces touch any of the various heatsinks on the PET printed circuit board. This is particularly critical on the old style PET's which have two heatsinks which will short against the board unless prevented from doing so.

If the external bus is to be used to connect to additional MTU boards, a K-1005-P card file will be needed. This card file is too large to fit inside the PET so it and the K-1008-6 will sit on the right side of the PET. The K-1008-6 should be plugged into the top slot of the card file to maximize the effective length of cable since it will have to come up and over the card file edge.

OPERATION

The K-1008-6 Integrated Visible Memory actually performs a number of functions and each of these are under software and jumper control. First of course it is an 8K Visible Memory useful for graphics and PET memory expansion. Next there are 5 ROM sockets which can hold a variety of preprogrammed ROM's from several manufacturers. A KIM expansion bus is available for further expansion using our motherboard/card file and other KIM-compatible MTU expansion boards. Finally there is a light pen register option that may be used in conjunction with a light pen for the input of graphic data. All of these functions must be understood to be effectively programmed and used.

VIDEO CONTROL REGISTER

The video control register is at location 49151 (BFFF in hex) in the PET's memory address space. By POKEing different values into it, it is possible to select Visible Memory video, regular PET video, an overlayed combination, or a blank screen. The various POKE statements are listed below:

POKE 49151,1	Select regular PET video
POKE 49151,2	Select Visible Memory video
POKE 49151,3	Select both which gives an overlayed (logical OR) image
POKE 49151,0	Blanks the screen without erasing it

In addition, a PET reset, such as turning power off then on, or a K-1008-6 reset will automatically select regular PET video only. There is no restriction in rapidly selecting different display modes and there will be no screen bounce or other interference when the video modes are switched. The video control register at BFFF (actually any address from BF00 - BFFF will work) is a write-only register so there is no harm if ROM occupies the same addresses.

ENABLE CONTROL REGISTER

In order to provide the maximum usefullness with the 32K new style PETs, The K-1008-6 has a bank switching feature that allows more than one memory "device" to share the same address space. The enable control register is used to determine which "device" is enabled to respond to addresses at a particular time. The K-1008-6 has 8 different devices, each of which corresponds to a bit in the enable control register as listed below:

DEVICE	CONTROL REG VALUE	BIT NO.
External KIM bus	1	0
Lower half of Visible Memory (top half of screen)	2	1
Upper half of Visible Memory (bottom half of screen)	4	2
ROM socket 1	8	3
ROM socket 2	16	4
ROM socket 3	32	5
ROM socket 4	64	6
ROM socket 5	128	7

The address of the enable control register is 48895 (BEFF) and the value POKEd there determines the mix of devices enabled. If more than one device is to be enabled, the POKE value is the sum of their control register values listed above. Thus to enable the Visible Memory and disable everything else, a POKE 48895,6 would be executed. Like the video control register, the enable control register is write-only so it may overlap ROM addresses with no ill effect. Note that disabling the Visible Memory does not affect display of the stored image; it merely inhibits reading or writing through the PET bus.

Each of the 8 devices listed above may be independently addressed on 4K boundaries with jumpers. Thus it is perfectly feasible to have more than one at the same address which is the key to the configuration flexibility of the K-1008-6. However it is important that only one device at a given address be enabled at a time so that they do not fight on the bus when enabled. Although the risk of electrical damage from a bus fight is essentially zero, the noise created might cause a program crash or alteration of memory contents.

Associated with the enable control register is a set of jumpers that defines the default enable after a PET or K-1008-6 reset. When the reset occurrs, the default configuration is automatically written into the enable control register in order to return the system to a standard configuration even if due to a software crash the desired value is not written there by software. With the standard jumper configuration, a 56 is written (ROM sockets 1-3 enabled, everything else disabled) after a reset. A set of 8 jumpers is provided to change the default configuration to anything desired. See the Jumper Options section for further details.

ROM SOCKETS

The 5 ROM sockets are provided to allow the use of available ROM software such as The Programmer's Toolkit, Commodore Word Processor, and others in systems with 32K of memory and the K-1008-6. It even allows incompatible ROM's (i.e. those that occupy the same addresses) to be in the system simultaneously although only one should be enabled at a time. When the ROM enable jumper in the PET is cut (which is recommended for 32K PET's and is required for VM addressing above the PET's screen addresses), any ROM's in the spare PET sockets will have to be removed and plugged into the ROM sockets on the K-1008-6. The correspondance table shows the K-1008-6 ROM assignments with the standard jumper configuration:

PET ROM LOCATION	K-1008-6 ROM LOCATION	ADDRESS RANGE	ENABLE REG	DEFAULT
D3	ROM 1	9000-9FFF	8	ON
D4	ROM 2	A000-AFFF	16	ON
D5	ROM 3	B000-BFFF	32	ON
D3	ROM 4	9000-9FFF	64	OFF
D4	ROM 5	A000-AFFF	128	OFF

Thus if the ROM's currently installed in locations D3 - D5 in the PET (if any) are removed and transferred to ROM sockets 1 - 3 respectively in the K-1008-6, then after a reset, the operation of the PET should be unchanged with respect to auxiliary ROM software. Note that the address range and default enable of all 5 of the ROM sockets may be changed by altering jumpers on the K-1008-6 board.

The ROM sockets on the K-1008-6 are designed to hold standard 4K byte mask programmed ROM's known by the generic number 2332. EPROM's such as the 2716 or 2732 cannot be used because both chip select pins (20 active-low and 21 active high) of the 2332 are used to select the ROM.

LIGHT PEN REGISTER

The light pen feature, when installed (4 type 74LS173 IC's must be installed in sockets U1-U4 and a jumper installed between pins 4 and 13 of U31 to make the feature operable), will latch the current dot address when triggered by a negative-going edge at the light pen input. The contents of this latch may be read at VM high address plus 4094 (least significant half) and VM high address plus 4095 (most significant half). Thus with the standard jumper configuration that puts the VM high address at 40960 (A000), the lower light pen byte may be accessed with a PEEK(45054) while the higher byte may be accessed with a PEEK(45055).

The X and Y coordinates (assuming that the 320 wide by 200 high graphic matrix is entirely in the first quadrant and 0,0 is the lower left corner) of the light pen register may be determined by executing the following BASIC statements:

```
LA=256*PEEK(45055)+PEEK(45054)
Y=INT(LA/320)
X=LA-320*Y
Y=199-Y
```

Although the light pen register identifies a particular pixel, it would require a very good light pen indeed (and well focused monitor) to actually be able to resolve a single pixel. In practice, the values read from the light pen register will vary a few units either way each vertical scan of the screen providing the light pen is actually picking up light from the screen. In fact, since there is no light pen "hit" flag, a light pen detect routine should wait until there is some change in the register contents before returning a new pair of coordinates to the calling program.

EXTERNAL KIM BUS

The K-1008-6 provides an edge connector with pinout similar to that on the expansion connectors of KIM-1, SYM-1, and AIM-65 single board computers. In addition, unregulated +8 and +16 volt power is provided on pins MTU has reserved for that purpose. When the K-1008-6 is plugged into one of our K-1005-P card files, up to 4 additional MTU expansion boards may also be plugged in. This feature is most useful with the smaller 8K and 16K PET's because memory expansion can then be accomplished with our K-1016 16K RAM board. If programmable ROM (up to 12K of inexpensive, readily available 2708 type EPROM) or numerous additional parallel ports are required, our K-1012 PROM/IO board will provide it. The K-1020 can be used for custom designed interfaces to the PET. Also our K-1013 disk controller/16K RAM is interfaced to the PET in this manner. If it is desired to feed external CCTV monitors with Visible Memory graphics, even a K-1008 Visible Memory can be plugged into the card file. If it is addressed at the same location as the Visible Memory on the K-1008-6 (see Jumper Options), then anything written into the K-1008-6 will also be written into the K-1008 and appear on the external monitors. It is even possible to use multiple K-1008's for 320x200 gray scale graphics with an external monitor (the PET's internal monitor cannot display shades of gray).

Unlike the 4K block size of the other 7 "devices" on the K-1008-6, the external bus has a block size of up to 32K according to what is plugged into it. The external bus is "disabled" by setting Address bit 15 high when bit 0 of the enable control register is set to a zero. Therefore, no boards on the external KIM bus should respond to addresses between 8000 and FFFF. Also, no boards on the external bus should respond to addresses that the PET internal memory responds to or other simultaneously enabled devices on the K-1008-6 respond to.

PET addresses are translated somewhat in conversion to KIM addresses on the external bus. The translation listed below is that provided with the standard K-1008-6 jumper configuration:

PET ADDRESS	KIM ADDRESS	PET ADDRESS	KIM ADDRESS	NOTES
0000-0FFF	F000-FFFF	8000-8FFF	F000-FFFF	1. Can be altered by jumper change.
1000-1FFF	F000-FFFF	9000-9FFF	F000-FFFF[1]	
2000-2FFF	0000-0FFF	A000-AFFF	6000-6FFF[1]	
3000-3FFF	1000-1FFF	B000-BFFF	7000-7FFF[1]	2. When ext. bus is disabled, all PET addresses are translated to Fxxx.
4000-4FFF	2000-2FFF	C000-CFFF	F000-FFFF	
5000-5FFF	3000-3FFF	D000-DFFF	F000-FFFF	
6000-6FFF	4000-4FFF	E000-EFFF	F000-FFFF	
7000-7FFF	5000-5FFF	F000-FFFF	F000-FFFF	

PROGRAMMING

Programming of the K-1008-6 to display text and graphics is very straightforward. The display is essentially a matrix of dots with 200 rows of 320 dots per row. For addressing purposes the dots can be numbered from 0 to 63,999 with dot 0 being the upper left-hand corner dot, dot 319 being at the upper right corner, dot 320 being the leftmost dot on the next row down, and 63,999 being the lower right-hand corner dot. Eight horizontally adjacent dots make up one byte of memory with the position of the dots on the display corresponding to the position of the bits in the byte. Thus dot 0 is the leftmost bit (bit 7, weight of 128) of the first byte in the Visible Memory. Conversely dot 319 would be the rightmost bit (bit 0) of the fourtieth byte.

POINT ADDRESSING

Usually graphics programming is performed using the X-Y method of identifying a particular dot position. Although the origin of the coordinate system can be assumed to be anywhere, it is convenient to place it at the lower left corner of the display. Thus all of the displayable points are in the first quadrant and X and Y are always positive numbers. To convert from X-Y point coordinates to a dot number is a simple matter involving evaluation of the equation: DOT # = (199-Y)*320+X . Conversion from the dot number to a byte address and bit number (assuming most significant bit is bit 0) is as follows: BYTE ADDR = VM BASE ADDR + INT(DOT #/8); BIT # = REM(DOT #/8) . Going directly from coordinates to byte address and bit number is as follows: BYTE ADDR = VM BASE ADDR + (199-Y)*40+INT(X/8); BIT # = REM(X/8) = X-8*INT(X/8). Note that the multiplication by 40 in machine language can be accomplished in steps as follows: A*40=(A+A*4)*8 where multiplication by 4 and 8 is accomplished by shifting left 2 and 3 positions respectively. Divison by 8 is accomplished by shifting right 3 positions.

GRAPHIC SUBROUTINE PACKAGE

Once the byte and bit addresses are found, the dot may be turned on with the logical OR instruction and turned off with an AND instruction or their BASIC equivalents. It is convenient to write subroutines that accept X and Y coordinates as input and set, reset, flip, write, or read a dot. These would in turn call a subroutine to compute the byte and bit addresses from X and Y coordinates. A more sophisticated subroutine would accept the coordinates of the endpoints of a line and fill in the points forming the closest approximation to the straight line between them. Characters may be drawn either as line segments or a dot matrix by using a font table and calls to the appropriate routine. In special cases drawing speed may be greatly increased by handling the 8 dots in a byte simultaneously.

Very simple BASIC subroutines to clear the screen and plot points are given on the next page and while they get the job done, they are very slow. The same functions performed in machine language are about 100 times faster.

AVAILABLE SOFTWARE

Although it is a lot of fun to build up graphic subroutines yourself, it is possible that some users would prefer to have the work done for them. A set of utility routines written in machine language but callable from BASIC is available as the K-1008-3C software package. Besides high speed screen clear and point plotting, they also do point erase, line plotting given X and Y endpoints, and text plotting up to 22 lines of 53 characters each; 13 more than the PET screen itself provides. Alternatively, text may be printed in the normal way on the PET screen and the overlay video option (POKE 49151,3) used to show the graphics and text overlayed. The two images will overlay with each PET character requiring a space of 8X by 8Y dots.

Diagnostic Program

```
10 REM  K-1008-6 VISIBLE MEMORY SIMPLIFIED DIAGNOSTIC
20 REM  TYPE RUN FOR THE VISIBLE MEMORY ADDRESSED AT 9000
30 REM  CHANGE LINE 100 IF STARTING ADDRESS IS OTHER
40 REM  THAN 9000 HEX
100 SA=9*4096
110 NL=8190: REM DO NOT TEST LIGHT PEN LOCATIONS
120 POKE 48895,6: REM ENABLE VISIBLE MEMORY, DISABLE ALL OTHER
200 FOR I=1 TO 10: REM 10 PASSES THROUGH DIAGNOSTIC
210 SD=RND(1): REM GET RANDOM SEED
220 Z9=RND(-SD)
300 FOR J=SA TO SA+NL-1: REM STORE RANDOM PATTERN IN MEMORY
310 POKE J,RND(1)*256
320 NEXT J
390 Z9=RND(-SD): REM RESTART RANDOM SEQUENCE
400 FOR J=SA TO SA+NL-1: VERIFY MEMORY CONTENTS
410 CT=PEEK(J)
420 RN=INT(256*RND(1))
430 IF CT=RN GOTO 450
440 PRINT 'ERR ADDR';J,'READ';CT,'WROTE';RN
450 NEXT J
500 PRINT 'PASS';I;'COMPLETED'
510 NEXT I
520 POKE 48895,56: REM RESTORE STANDARD ENABLE CONFIGURATION
530 STOP
```

Point Plot Demonstration Program

```
10 REM VISIBLE MEMORY POINT PLOT DEMONSTRATION PROGRAM
20 REM TYPE RUN TO GET A PLOT OF A SINE WAVE
30 REM CHANGE LINE 100 IF STARTING ADDRESS IS OTHER
40 REM THAN 9000 HEX
100 SA=9*4096
110 POKE 49151,2: REM SWITCH TO VISIBLE MEMORY DISPLAY
120 POKE 48895,6: REM ENABLE VISIBLE MEMORY, DISABLE ALL OTHER
130 GOSUB 1000: REM CLEAR VISIBLE MEMORY
200 FOR X1=0 TO 319
210 Y1=99*SIN(6.28318*X1/320)+100
220 GOSUB 2000: REM PLOT POINT AT X1,Y1
230 NEXT X1
240 FOR I=1 TO 5000: NEXT I
250 POKE 49150,1: REM SWITCH TO PET VIDEO
260 POKE 48895,56: REM RESTORE STANDARD ENABLE CONFIGURATION
270 STOP
1000 REM CLEAR VISIBLE MEMORY AS FAST AS POSSIBLE WITH BASIC
1010 ZR=0
1020 TM=SA+7999
1030 FOR I=SA TO TM: POKE I,ZR: NEXT
1040 RETURN
2000 REM PLOT POINT AT X1,Y1  0<=X1<320  0<=Y1<200
2010 AD=40*INT(199-Y1)+INT(X1/8)+SA
2020 BT=2↑(7-(X1 AND 7))
2030 POKE AD,(PEEK(AD) OR BT)
2040 RETURN
```

SYSTEM CONFIGURATION

Most people have their own ideas about how a computer system should be configured. The following are merely suggestions as to the most effective ways to configure a PET, K-1008-6 interface, and various K series MTU boards. An almost infinite variety of variations are possible. Note that all MTU boards are address selectable by jumpers.

First a number of questions will be asked in order to characterize the needs and goals of the customer. Then the answers will be used as a guide to selecting one of the configuration options listed later.

1. Do you have an old PET (new or old ROM's) or a new PET or CBM? ___
2. How much internal memory does your PET have (8K, 16K, or 32K)? ___
3. Is it a requirement to be able to utilize the 8K of memory on the K-1008-6 as additional program storage when not using graphics? ___
4. If you have a new PET, are you comfortable in altering the internal PET jumpers? ___
5. If you have a new PET, are you or do you contemplate using an accessory ROM such as the word processor or Programmer's toolkit? ___
6. If the answer to 5 is Yes, do you contemplate using more than three accessory ROM's or two ROM's with conflicting addresses? ___

Only a few of the nearly 100 possible combinations of answers will be listed below. Choose the one that most nearly meets your needs. An * as a response indicates that the answer is irrelevant given the answers to the other questions.

1-New 2-32K 3-* 4-Yes 5-* 6-*	Use the standard K-1008-6 jumper configuration
1-New 2-32K 3-* 4-No 5-Yes 6-No	Use the standard K-1008-6 jumper configuration except put video memory low at 6000 and video memory high at 7000. BASIC programs using graphics will be restricted to 24K.
1-New 2-* 3-* 4-No 5-Yes 6-Yes	This combination cannot be accomodated. You must either alter the PET jumpers or restrict ROM usage to 3 ROM's at different addresses
1-New 2-16K 3-Yes 4-Yes[1] 5-* 6-*	Use the standard K-1008-6 jumper configuration except put video memory low at 4000 and video memory high at 5000.
1-New 2-8K 3-Yes 4-Yes[1] 5-* 6-*	Use the standard K-1008-6 jumper configuration except put video memory low at 2000 and video memory high at 3000.
1-Old 2-8K 3-* 4-* 5-* 6-*	Use the standard K-1008-6 jumper configuration except put video memory low at 2000 and video memory high at 3000.

NOTES: 1. Some PETS left the factory with the jumpers set for 32K of internal memory even though that much was not installed. For these, the jumpers will have to be changed, otherwise not. Check the configuration against those listed on page 4.

JUMPER OPTIONS

Because of the wide variety of PET and CBM configurations and variations in personal taste, there are a number of configuration jumpers on the K-1008-6 board. In order to simplify, or possibly eliminate, the task of configuring the board for the user's system, the board is shipped with a "standard" jumper configuration that should be suitable for the largest number of users. This standard configuration is listed on page 1 and is also designated with an * in the jumper option tables in this section. There are three classes of jumpers: address selection, default enables, and miscellaneous. Each of these will be described in detail in the following paragraphs.

ADDRESS SELECTION JUMPERS

Each of the 8 "devices" on the K-1008-6 board has its own set of address selection jumpers. Although not every possible PET address is available for each device, there should be sufficient flexibility to set up any reasonable configuration. The jumpers themselves are small staple-shaped pieces of wire with white insulation and chisel pointed ends. They may be repeatedly plugged into and removed from the jumper sockets without harm. There should be enough jumpers supplied with the board to support any desired reconfiguration. Alternativly, DIP switches may be installed if frequent reconfigurfation is anticipated.

Video Memory Low
(upper half of screen)

2000-2FFF	U11-8 to U11-9
3000-3FFF	U11-7 to U11-10
4000-4FFF	U11-6 to U11-11
5000-5FFF	U11-5 to U11-12
6000-6FFF	U11-4 to U11-13
7000-7FFF	U11-3 to U11-14
9000-9FFF	U11-2 to U11-15 *
A000-AFFF	U11-1 to U11-16

Video Memory High
(lower half of screen)

3000-3FFF	U5-8 to U5-9
4000-4FFF	U5-7 to U5-10
5000-5FFF	U5-6 to U5-11
6000-6FFF	U5-5 to U5-12
7000-7FFF	U5-4 to U5-13
9000-9FFF	U5-3 to U5-14
A000-AFFF	U5-2 to U5-15 *
B000-BFFF	U5-1 to U5-16

ROM 1 Address

3000-3FFF	U14-8 to U14-9
4000-4FFF	U14-7 to U14-10
5000-5FFF	U14-6 to U14-11
6000-6FFF	U14-5 to U14-12
7000-7FFF	U14-4 to U14-13
9000-9FFF	U14-3 to U14-14 *
A000-AFFF	U14-2 to U14-15
B000-BFFF	U14-1 to U14-16

ROM 2 Address

7000-7FFF	U15-4 to U15-13
9000-9FFF	U15-3 to U15-14
A000-AFFF	U15-2 to U15-15 *
B000-BFFF	U15-1 to U15-16

ROM 3 Address

7000-7FFF	U15-8 to U15-9
9000-9FFF	U15-7 to U15-10
A000-AFFF	U15-6 to U15-11
B000-BFFF	U15-5 to U15-12 *

ROM 4 Address

7000-7FFF	U16-4 to U16-13
9000-9FFF	U16-3 to U16-14 *
A000-AFFF	U16-2 to U16-15
B000-BFFF	U16-1 to U16-16

ROM 5 Address

7000-7FFF	U16-8 to U16-9
9000-9FFF	U16-7 to U16-10
A000-AFFF	U16-6 to U16-11 *
B000-BFFF	U16-5 to U16-12

External KIM Bus

External KIM bus addresses 0000-5FFF are permantly assigned to PET addresses 2000-7FFF respectively. The two remaining 4K blocks on the external bus may be assigned to any two of the three remaining PET 4K blocks either 9000-9FFF, A000-AFFF, or B000-BFFF. Note that the jumpers do not necessarily go striaght accross the jumper socket so DIP switches cannot be used to control this option.

PET 9000-9FFF = BUS 6000-6FFF	U31-1 to U31-16
PET A000-AFFF = BUS 7000-7FFF	U31-2 to U31-15
PET 9000-9FFF = BUS 6000-6FFF	U31-1 to U31-16
PET B000-BFFF = BUS 7000-7FFF	U31-3 to U31-15
PET A000-AFFF = BUS 6000-6FFF	U31-2 to U31-16 *
PET B000-BFFF = BUS 7000-7FFF	U31-3 to U31-15 *
PET 9000-9FFF = BUS 7000-7FFF	U31-1 to U31-15
PET A000-AFFF = BUS 6000-6FFF	U31-2 to U31-16
PET 9000-9FFF = BUS 7000-7FFF	U31-1 to U31-15
PET B000-BFFF = BUS 6000-6FFF	U31-3 to U31-16
PET A000-AFFF = BUS 7000-7FFF	U31-2 to U31-15
PET B000-BFFF = BUS 6000-6FFF	U31-3 to U31-16

DEFAULT ENABLE JUMPERS

An installed jumper will disable a device on power-up or reset.
An omitted jumper will enable a device on power-up or reset.

External BUS	U34-8 to U34-9 *
Visible Memory low	U34-7 to U34-10 *
Visible Memory high	U34-6 to U34-11 *
ROM Socket 1	U34-5 to U34-12
ROM Socket 2	U34-4 to U34-13
ROM Socket 3	U34-3 to U34-14
ROM Socket 4	U34-2 to U34-15 *
ROM Socket 5	U34-1 to U34-16 *

MISCELLANEOUS JUMPERS

If the light pen register IC's are NOT installed in the board, the last two locations of the Visible Memory may be made usable for storage by removing the jumper between U31-4 and U31-13. If the registers are installed, removing this jumper will cause an on-board conflict between the memory and the register.

Due to differences in video timing between old and new PET's, there is a jumper that will optimize the overlay of Visible Memory video and PET video.

OLD PET	U31-7 to U31-10
NEW PET	U31-8 to U31-9 *

PRINCIPLES OF OPERATION

The K-1008-6 Integrated Visible Memory for the PET computer is basically a combination of our K-1007-P to MTU bus adaptor and our K-1008 Visible Memory. Additional circuitry has been added to provide 5 ROM sockets, a light pen register, and video synchronization to the PET.

ADDRESS RECOGNITION

The left side of page 1 of the schematics contains most of the address recognition circuitry on the board. U5 is a jumper socket that selects which of the PET SEL lines is to activate the upper 4K of the graphic memory addresses (VM HIGH) These SEL lines are simple 1-of-16 decodings of the upper 4 address bits from the 6502 microprocessor in the PET. Thus SEL4 will go to a logic low when any address in the range of 4000-4FFF appears on the address bus while the other SEL lines remain high. U11 is a similar jumper socket for the lower 4K of the graphic memory (VM LOW). U14 is a jumper socket to select the address for ROM-1 (CE ROM 1) which can be any of the PET 4K blocks except 2000-2FFF. U15 and U16 are each split into two halves to select addresses for ROM-2 through ROM-5 (CE ROM 2, CE ROM 3, CE ROM 4, and CE ROM 5). Each of the resulting 7 address selections are ANDed with corresponding bits in the Enable Register to produce enables for the graphic memory and ROM sockets.

The KIM bus address encoder is at the upper left of page 1. A type 74148 priority encoder IC is used to re-encode the PET's SEL lines back into 4-bit binary for the KIM bus. The highest two inputs to the encoder can be jumpered to any two of SEL 9, SEL A, or SEL B. The external bus is turned on and off by connecting the EI pin of the 74148 to bit zero of the Enable Register. When EI is high, the encoder puts out an F irregardless of the other inputs and since no boards on the KIM bus should respond Fxxx addresses, the external bus is effectively disabled.

Additional address decoding is at the upper left corner of page 3. This circuitry recognizes addresses assigned to the Enable Control register, Video Control register, and Light Pen registers. OPTION WRITE is the clock to the Enable Control register which goes low during Phase 2 of write cycles when the address bus has BExx on it. U47 detects this condition by NANDing SEL B, PHASE 2, READ/WRITE, A11, A10, A9, and A8 together and generating OPTION WRITE when they are coincident. VIDEO CONTROL CLK is the clock to the Video Control register which goes low during Phase 2 of write cycles when the address bus has BFxx on it. U28-8 goes low when A8, A9, A10, and A11 are all high and this is then inverted to a high by U58-2. U28-6 senses the coincidence of the previous condition, SEL B, READ/WRITE, and PHASE 2 and generates VIDEO CONTROL CLK. The light pen address recognition circuitry detects the next to last address in the video memory to generate LP REG LB which allows reading the low byte of the light pen register, and detects the last address in the video memory to generate LP REG HB for reading the high byte. The signal from U58-2, which represents addresses xFxx, is combined with the signal from U6-8, which represents addresses xxFE or xxFF, and VM HIGH in U48-12 to form a signal that goes low when either light pen register is addressed. U39-3 and 11 distinguishes which ligh pen register is actually addressed based on A0. The net result is LP REG LB going low when the low light pen byte is addressed and LP REG HB going low when the high light pen byte is addressed. These two signals and then logically OR'ed together by U33-8 to generate LIGHT PEN ADRD. (U48-8 could just as well have been used for this signal but it was not).

At the lower right corner of page 1 is logic that OR-combines all of the address recognition signals in order to enable the data out drivers to the PET bus. U30 responds if anything on the board is addressed (except the two control registers). U29-11 responds if either half of the video memory is addressed and generates the VM SELECTED signal. U20-11 responds if anything is addressed except that LIGHT PEN ADRD is factored in to inhibit generation of MEM if the light pen enable jumper is in place. This is required in order to preven the memory data buffers from fighting against the light pen registers when the latter are read.

ROM SOCKETS

The five ROM sockets are on the right side of page 1. Basically the five sockets are wired in parallel with the lower 12 address lines, the 8 data lines, and power strictly in parallel. Since the type 2332 ROM has two chip selects, one is used to actually select a ROM from the CE ROM 1 through CE ROM 5 signals while the other is used to gate the data out only during PHASE 2. Data may not be gated out during PHASE 2 since it would interfere with data being read from the video memory during PHASE 2 and thus generate snow on the screen and excessive noise on the board. As a result, any ROM used in these sockets must have two chip select lines; one active-low on pin 20, and the other active high on pin 21.

BUS SIGNAL BUFFERING

The top right corner of page 1 has logic which buffers and processes some of the PET bus control signals for use by the K-1008-6 on-board logic as well as the external KIM/MTU bus. READ/WRITE is inverted by U19-6 to provide READ/WRITE. RESET is inverted by U19-4 to provide RESET. PHASE 2 is inverted by U19-8 to provide PHASE 2. U20-3 combines PHASE 2 and READ/WRITE together to provide RAM R/W, which goes low during Phase 2 of write cycles, to the external KIM/MTU bus.

The far left portion of page 2 contains the data bus buffers for data read from the video memory and the five ROM sockets. U43 and U63 are 4-bit latches with tri-state outputs which perform the data buffering function. The registers are set to latch whatever is on the D0-D7 internal data bus approximately 2/3 of the way through Phase 2. The register contents are gated onto the PET data bus (DATA 0 - DATA 7) during read cycles when MEM is low. The light pen registers (U1 - U4) at the upper right of page 3 are also tri-state latches which gate their data directly onto the PET data bus during read cycles when LP REG LB (U2 and U2) is low or when LP REG HB (U3 and U4) is low.

At the lower left corner of page 2 are data in buffers for the video memory. Since the memory chips used invert the data written into them, these buffers invert the data going in so that data read out will be correct. U52-4, 6, 8, 10 and U72-4, 6, 8, 10 perform this buffering and inversion function.

ENABLE CONTROL REGISTER

The Enable Control Register is in the bottom right section of page 2. U22 and U25 are specialized 4 bit registers that have an internal 4-wide 2-input multiplexor on the register inputs. One set of inputs is used for writing into the register under PET software control. The other set is used to write the default enable configuration from the jumpers when the board is reset. The logic at the bottom of the page is used to control writing of the default configuration. When OPTION WRITE goes low, it simply passes through U20-8 and clocks the registers. Since reset is not active at this time, U33-6 is high which selects the 1 inputs to the multiplexors and thus data from the PET bus. When reset goes active and then releases, the registers are also clocked through U20-8 but now the 0 multiplexor inputs are selected since R2 and C22 maintain a low level at U22-10 and U25-10 momentarily until the registers are clocked. The circuitry around U71 allows a user supplied switch to reset the board without turning the PET power off.

VIDEO CONTROL REGISTER

The video control register is at the top left corner of page 3. It is simply two J-$\overline{K}$ flip-flops (U40) connected as a D-type flip-flop. These form a two bit register that latches the state of DATA 0 and DATA 1 on the trailing edge of VIDEO CONTROL CLOCK which pulses low when write cycles to address FFxx are executed. The top flip-flop, which is controlled by DATA 1 turns the graphic video on when it is set. The bottom flip-flop, which is controlled by DATA 0 turns the PET video on when it is set. BOARD RESET insures that the flip-flops are set for graphic video off and PET video on at power-up or when the optional reset button is pressed.

TIMING GENERATOR

The upper left corner of page 3 contains the memory cycle timing generator and video clock circuitry. All of the board's timing is derived from an 8mHz oscillator which is phase-locked to the rising edge of PHASE 2 from the PET. Each cycle of this oscillator represents 1 dot on the display which is also 125 NS. The output of the oscillator in turn drives a three bit counter (U62-3, 4, 5) which is then decoded to provide timing signals for the board.

U71-8 is the voltage controlled oscillator in the phase locked loop which is just a classic Schmidt trigger R-C oscillator. The 500 ohm pot (R18) determines the oscillator's free-running frequency and is set for a nominal frequency of 8.0mHz. This simple oscillator is made to act as a voltage controlled oscillator (VCO) by connecting a resistor (2.2K) to the R-C node. Changes in current through this resistor caused by voltage changes at its free end affect the oscillator's frequency. Although the linear VCO range is only 20% or so, this is ample for locking to a fixed crystal- controlled frequency.

The phase detector is also rather unique. Since the phase angle of the lock between the on-board oscillator/counter chain and the 6502's PHASE 2 clock affects data transfer timing, it had to be controlled more tightly than a typical exclusive-or phase detector would provide. A tri-state buffer (U21) is used to do this A 250NS pulse at a 1.0mHz rate from the first three stages of the counter chain enables the tri-state buffer. The data input to the buffer is PHASE-2 from the PET. Ideal timing for data transfer between PET and K-1008-6 occurs when the trailing edge of PHASE 2 occurs midway in the enable pulse. Under these conditions the output of the buffer floats for 3/4 of the cycle, is driven high for about 1/8 of the cycle, and then is driven low for the remaining 1/8 of the cycle before floating again. This wildly gyrating buffer output voltage is averaged by the low pass filter formed by R21 and C103. If PHASE 2 turns off earlier in the enable window, the buffer output high time becomes less than the low time and the low-pass filter output voltage decreases thus speeding up the VCO which corrects for the error. The converse is true if PHASE 2 becomes late. The exact equilibrium point can be changed by adjusting the 500 ohm pot, R18. Normally R18 is adjusted at the factory and then sealed. If U71 or any of the discrete parts around it are changed, it will be necessary to readjust U71. See the troubleshooting section for an adjustment procedure.

Several timing signals are derived from the 3 bit counter, U62. The counter bits themselves are called DOT1, DOT2, and DOT4. The 25% duty cycle enable pulse for the phase detector is generated by ANDing DOT2 and DOT4 together in U39-6. U48-6 generates s signal called DOT7 which goes low when DOT1, DOT2, and DOT4 are all high. This signal represents the end of a video byte time and is used to load the next 8 dots into the video shift register. U60-10 and surrounding logic is used to generate the clock signal, MEMCE, for the dynamic RAM chips used in the video memory.

MEMORY CLOCK DRIVERS

MEMCE goes through additional gating in U67 and U76 before entering the high--level clock drivers. The purpose of this gating is to clock the RAM chips only when necessary in order to save power. The upper set of AND inputs to each gate are associated with PET cycles into the video memory. A clock pulse passes only when VM SELECTED is true and DOT4 is false which is nearly coincident with PHASE 2. The RAM row that is actually clocked is determined by the state of ADDR 0. The lower set of AND inputs to each gate are associated with video cycles into the video memory. A clock pulse pases only when VIDEO ACCESS is true and DOT4 is true which is nearly coincident with PHASE 2. The RAM row that is actually clocked is determined by the state of DISP AD 0.

The clock driver itself is built with discrete components. Its purpose is to generate a fast rise and fall signal of 12 volts in amplitude capable of driving a heavy capacitive load. The inactive state of the clock is low which can be maintained indefinitely by direct coupling to NPN transistors Q2 and Q4 from the clock gates. When a clock pulse is required, the NPN transistor is driven off and the PNP transistor driven on by coupling through a 220pF capacitor to its base. The PNP then pulls the clock line high and can keep it high for the 300NS duration of the clock pulse. The clock drivers are not protected against short circuits to the +12 supply. If any of the transistors need to be replaced, they should be replaced with the same type number. Substitutes are likely to be too slow for proper operation.

RAM ARRAY

Page 5 shows the video RAM array. The RAM's are of the 22 pin 4K dynamic variety and are arranged into two rows of 8 each to provide 8192 bytes of storage. The top row of chips is assigned to even addresses while the bottom row is assigned to odd addresses. Row selection is done via the clock lines rather than the chip select lines in order to save power. Even/odd addressing is used so that refreshing can be performed automatically by the video scanning logic.

VIDEO GENERATION AND CONTROL

The most complex logic on the board is associated with video synchronization and generation. The PET display logic actually generates three video-related signals which are called P VERT, P HORIZ, and P VIDEO. The first two are vertical and horizontal drive signals used by the sweep circuitry in the PET's display monitor. P VIDEO contains the actual video signal representing the PET's normal character and limited graphics display.

The on-board graphic video generator synchronizes itself with $\overline{\text{P VERT}}$ and P HORIZ and then generates its own graphic video called VM VIDEO. The display monitor always receives horizontal and vertical drive directly from $\overline{\text{P VERT}}$, and P HORIZ but the video goes through a gating network at the top left corner of page 2. $\overline{\text{P VIDEO}}$ is first inverted by U32-4 and then gated with PET VIDEO ON in U20-6. It is then ORed with VM VIDEO in U33-3. VM VIDEO ON gates VM VIDEO elsewhere in the circuitry. The net result is the ability to select P VIDEO, VM VIDEO, both, or neither.

VM VIDEO is generated by a parallel load serial out shift register, U78. The 8mHz DOT CLK is constantly shifting the register contents however when $\overline{\text{VM SR LOAD}}$ is active (low), the register parallel loads rather than shifts, on the next clock pulse. Normally the register is loaded with new data every microsecond at DOT7 time. If it is not loaded, the zeroes being shifted in constantly will start coming out which is a black video level. Thus blanking for horizontal and vertical retrace is implemented by gating out $\overline{\text{VM SR LOAD}}$ pulses.

SWEEP SYNCHRONIZATION

The purpose of the horizontal synchronizer is to generate a gating signal to the video shift register and video memory address counter so that graphic video is horizontally coincident with PET video. HORIZ DRIVE (which is the same as P HORIZ) is first positive edge detected by U68 at the bottom right of page 4. This very narrow pulse (125NS) then clears the horizontal counters, U12-8 and U62-8. After clearing, these counters count up every microsecond on the trailing edge of DOT4 which occurrs at the same time as the trailing edge of DOT7 which is also at the same instant that the shift register is loaded with the next 8 bits to display. Each horizontal sweep cycle is exactly 64 uS long. The gating network connected to the counters in conjunction with the flip-flop U49-6 generates a 40uS window, called VIDEO ACCESS, within the 64uS cycle during which graphic video is to be generated. U49-10 serves to delay VIDEO ACCESS by 1uS and a jumper is provided to select between delayed and undelayed to accomodate timing differences between old and new style PET's. The selected window is then used directly to control the display address counter and delayed by 500NS (U60-6) to control loading of the video shift register. During vertical retrace, U60-6 is held off to inhibit loading of the shift register and thus blank the graphic video.

The vertical synchronizer is at the top right corner of page 2. It too consists of a counter and gating network whose sole purpose is to generate a window for the graphic video generator. The P VERT signal goes low for 1.3 milliseconds which occurs during vertical retrace. P VERT is inverted and resets the U42 counters. When the reset is released, the counters count up on the leading edges of the P HORIZ signal. The gating network (U33-11, U32-2, U41-6, U48-8, and U50-2) in conjunction with U51 generate a window that is 200 counts wide. A full vertical cycle is 260 counts in duration. The window generated is then called VERT DISP ON which goes to page 4 to control the shift register loading and page 3 to control the display address counter.

DISPLAY ADDRESS GENERATOR

The display address generator is at the bottom left of page 3. It is a 13 bit counter made from a flip-flop and three 4-bit counters. It is reset at the beginning of the VERT DISP ON window via an edge detector (C66, R13, R14, and U50-8. It is counted by INC DISP ADDR which is generated at every DOT7 time during which VIDEO ACCESS is true. Note that the counter continues to count during the vertical blanking interval. This is necessary to keep the memory refreshed during the blanking interval which is longer than 2 milliseconds. U8, U9, and U10 are an address multiplexor which selects between PET addresses when DOT4 (essentially identical to PHASE 2) is low and display addresses when DOT4 is high.

LIGHT PEN

U69 is the schmidt trigger input for the light pen. R15 is provided so that a simple phototransistor can be used for the sensor (although the sensitivity and resolution will not be very good). U70 is used to synchronize the light pen signal with the video clock and U59-9 detects negative-going edges into the light pen input. The 125NS pulse from U59 clocks the 16 bit light pen register which latches the current 13 bit display address and 3 bit dot number.

POWER SUPPLY

The power supply is at the lower left corner of page 4. Unregulated PET DC is passed directly to the KIM/MTU bus and is regulated to +5 volts by VR2 to power K-1008-6 on-board logic. PET AC is voltage doubled by D1, D2, C7, and C10 to provide unregulated +16 volts to the bus and is regulated to +12 by VR1 to power the video memory. Negative 5 for the memory is also obtained from PET AC with D3 and C8 and regulated by R1 and 5.1 volt zener diode D4.

TROUBLESHOOTING

All K-1008-6 boards are actually tested on a PET computer before shipment so any problems are most likely due to shipping damage or incorrect installation While the connector boards and cables are not specifically tested, there is little to go wrong with them. If you believe that the problem is with the connector board (either K-1007-2 or K-1007-3) or the red ribbon cable, return them for repair or replacement. If the problem seems to be with the K-1008-6, please read the following paragraphs, which describe the most frequent problems, first.

CANNOT READ FROM THE K-1008-6

First be sure that the device you are trying to read from is enabled! See the section on operation for details. If the memory diagnostic fails and further checking reveals that the graphic memory cannot be read from and you have a new PET, the likely cause is the internal PET jumpers. If these are not set right, the PET bus buffers will not be activated and data from the K-1008-6 will not be gated in. Carefully inspect the jumpers (with a dentist's mirror and strong light if necessary) and certify that they are set as described in the new PET installation section. Also verify that the K-1008-6 jumpers are set for the addresses you are expecting.

If you cannot read from the light pen registers, verify that the light pen IC's are installed (they are an extra cost option) and that a jumper has been placed between pins 4 and 13 of socket U31.

If you cannot read from the on-board ROM sockets, again verify that the new PET jumpers are set correctly and that the ROM address select jumpers on the K-1008-6 are set for the desired addresses. Also verify that the ROM is plugged into the appropriate socket (they are not in sequential order on the board) and that the ROM is a 2332 type with pin 20 masked for an active-low chip select and pin 21 masked for an active-high chip select. The video control and enable control registers are write-only and cannot be read back.

SNOW ON THE GRAPHIC DISPLAY

The usual cause of this is not using a type 2332 ROM in the K-1008-6 ROM sockets or a ROM with inappropriate chip select masking. In particular, a type 2716 or 2732 EPROM cannot be used without additional gating since they have only one chip select.

CANNOT READ AUXILIARY ROM SOCKETS IN THE PET

The PET jumper change recommended for 32K new style PET's disables the PET auxiliary ROM sockets. The idea is to use the ROM sockets on the K-1008-6 for any auxiliary ROM's needed. If it is absolutely necessary to plug the ROM's into the PET rather than the K-1008-6 (for example, a 2716 or 2732 EPROM), then the PET jumper controlling the PET ROM sockets should not be disturbed and it will be necessary to address the graphic memory below the PET's screen. See the section titled System Configuration for options.

ADJUSTING THE DOT SYNC POTENTIOMETER

If the graphic video image is jittery and/or the display dots are randomly turning off and on and the memory test program gives random read data back, it is possible that the Dot Sync potentiometer has been tampered with. To adjust the pot, first select graphic video (POKE 49151,2) which should be jittery. Rotate R18 with a small screwdriver until the display is stable. Connect a voltmeter to the end of C103 that gives a non-zero reading and further rotate R18 until the voltage reads +1.5 volts. The display should remain stable. Finally run the memory test program to insure that the phase locked loop has not locked on a subharmonic of the Phase 2 clock.

K-1008-6 PARTS LIST

DESIGNATION ( )=LIGHT PEN OPTION	PART TYPE	QTY
U18,20,29,39	LOGIC,74LS00(14)	4
U17,19,32,(38), 50,52,58,72	LOGIC,74LS04(14)	7
U33,59	LOGIC,74LS08(14)	2
U48,61	LOGIC,74LS10(14)	2
U69,71	LOGIC,74LS13(14)	2
U28,41	LOGIC,74LS20(14)	2
(U6),30,47	LOGIC,74LS30(14)	2
U67,76	LOGIC,74LS55(14)	2
U40,49,51,60, 68,(70)	LOGIC,74LS109(16)	5
U13	LOGIC,74LS148(16)	1
U8,9,10	LOGIC,74LS158(16)	3
U78	LOGIC,74LS166(16)	1
(U1-4),43,63	LOGIC,74LS173(16)	2
U22,25	LOGIC,74298(16)	2
U21	LOGIC,74LS368(16)	1
U7,12,42,62	LOGIC,74LS393(14)	4
U23,24,26,27,35,36,44,45, 53-56,64,65,73,74	4K DYN MEMORY 22 PIN	16
D1,2,3	DIODE,1N4001	3
D4	DIODE,ZENER 5% .4W 5.1V	1
VR2	VOLTAGE REGULATOR,LM340T5	1
VR1	VOLTAGE REGULATOR,LM341P12	1
Q1,4	TRANSISTOR NPN,2N3646	2
Q2,3	TRANSISTOR PNP,2N4916	2
C8,9,11,12,102	CAP,ELECTROLYTIC 16V 100UF	5
C7	CAP,ELECTROLYTIC 16V 2200UF	1
C10	CAP,ELECTROLYTIC 25V 1000UF	1
C104	CAP,CERAMIC DISK NPO 68PF	1
C95,98	CAP,CERAMIC DISK Z5U 100PF	2
C66,94,97	CAP,CERAMIC DISK Z5U 220PF	3
C22	CAP,CERAMIC DISK Z5U 1000PF	1
C103	CAP,CERAMIC DISK Z5U .01UF	1
C1-6,13-21,23-65,67-93, 96,99-102	CAP,CERAMIC DISK Z5U .047UF	89
J52,53	CONN,HEADER 7 PIN (RESET/LIGHTPEN)	1
J1	CONN,HEADER 60 PIN RIBBON	1
R17	RESISTOR,1/4W 5% 10 OHM	1
R8,11	RESISTOR,1/4W 5% 27 OHM	2
R2	RESISTOR,1/4W 5% 270 OHM	1
R19,21	RESISTOR,1/4W 5% 470 OHM	2
R1,9,12	RESISTOR,1/4W 5% 1K	3
R7,10,20	RESISTOR,1/4W 5% 2.2K	3
R3-6,13,14,16	RESISTOR,1/4W 5% 10K	7
R15	RESISTOR,1/4W 5% 27K	1
RP1,2,3	RESISTOR,SIP,10K 7 RESISTORS	3
R18	TRIMPOT, CERMET 500 OHM	1
HVR1	HEAT SINK 1" SQUARE TO-220	1
HVR2	HEAT SINK 2" RECT. TO-220	1
ALL 14 PIN IC'S	SOCKET,PC,14 PIN	29
ALL 16 PIN IC'S & JUMPERS	SOCKET,PC,16 PIN	26
ALL RAM IC'S	SOCKET,PC,22 PIN	16
ALL ROM IC'S	SOCKET,PC,24 PIN	5
	CABLE, RIBBON 60 WIRE 1 FOOT	1
	BOARD,PC K1008-6	1

SPECIFICATIONS

MECHANICAL: K-1008-6 11" wide by 8 1/2" deep excluding edge fingers.
K-1007-2 4 7/8" wide by 3 1/2" deep including edge socket.
K-1007-3 5 1/2" wide by 2 1/4" deep.

CABLES: 60 pin 12" cable connects K-1008-6 to K-1007-2 or K-1007-3. K-1007-2 has three 18" wires for power and a 14" video cable. K-1007-3 has an 18" power cable and a 14" video cable.

POWER SUPPLY: Utilizes PET AC via the included cable to provide +8 volts unregulated and +16 volts unregulated to the external KIM/MTU bus and expansion boards. Maximum current available is .75 amps on the +8 volt output and .35 amps on the +16 volt output.

VIDEO CIRCUITS: Graphic generator provides a dot matrix 320 wide by 200 high, each dot corresponds to a byte in the 8K onboard RAM. Video sync circuity synchronize the graphic video with the PET video allowing glitchless switching or overlay. Access to PET video and video monitor inputs is via connectors and cables provided.

ADDRESSING: Video control register addressed at BFxx and enable control register addressed at BExx, both are write-only and thus do not interfere with the use of these addresses for ROM. Graphic memory may be addressed on any 4K boundary and must have 8K of contiguous addresses. Five ROM sockets independently jumper addressable in 4K blocks.

SOFTWARE PROVIDED: The manual contains a diagnostic program and a Visible Memory demonstration program listing, both written entirely in BASIC. A high speed machine language graphics software package that is callable from BASIC is available and is called the K-1008-3C.

OLD PET PIN CONNECTIONS (odd/even numbering)

All Even Numbers GROUND

1	ADDR 0	53	$\overline{\text{RESET}}$
3	ADDR 1	55	$\overline{\text{IRQ}}$
5	ADDR 2	57	PHASE 2
7	ADDR 3	59	READ/WRITE
9	ADDR 4	65	DATA 0
11	ADDR 5	67	DATA 1
13	ADDR 6	69	DATA 2
15	ADDR 7	71	DATA 3
17	ADDR 8	73	DATA 4
19	ADDR 9	75	DATA 5
21	ADDR 10	77	DATA 6
23	ADDR 11	79	DATA 7
31	$\overline{\text{SEL 1}}$		
33	$\overline{\text{SEL 2}}$		
35	$\overline{\text{SEL 3}}$		
37	$\overline{\text{SEL 4}}$		
39	$\overline{\text{SEL 5}}$		
41	$\overline{\text{SEL 6}}$		
43	$\overline{\text{SEL 7}}$		
45	$\overline{\text{SEL 9}}$		
47	$\overline{\text{SEL 10}}$		
49	SEL 11		

NEW PET PIN CONNECTIONS (1-25, 26-50 numbering)
"A" connector toward back
A26-A50 and B26-B50 GROUND

A2	ADDR 0	B22	$\overline{\text{RESET}}$
A3	ADDR 1	A19	$\overline{\text{IRQ}}$
A4	ADDR 2	A21	PHASE 2
A5	ADDR 3	A22	READ/WRITE
A6	ADDR 4	B2	DATA 0
A7	ADDR 5	B3	DATA 1
A8	ADDR 6	B4	DATA 2
A9	ADDR 7	B5	DATA 3
A10	ADDR 8	B6	DATA 4
A11	ADDR 9	B7	DATA 5
A12	ADDR 10	B8	DATA 6
A13	ADDR 11	B9	DATA 7
NC	$\overline{\text{SEL 1}}$		
B10	$\overline{\text{SEL 2}}$		
B11	$\overline{\text{SEL 3}}$		
B12	$\overline{\text{SEL 4}}$		
B13	$\overline{\text{SEL 5}}$		
B14	$\overline{\text{SEL 6}}$		
B15	$\overline{\text{SEL 7}}$		
B17	$\overline{\text{SEL 9}}$		
B18	$\overline{\text{SEL 10}}$		
B19	SEL 11		

MTU BUS PIN CONNECTIONS (industry std. numbering)

A	ADDR 0	1	N.C.
B	ADDR 1	2	VM VIDEO
C	ADDR 2	3	N.C.
D	ADDR 3	4	$\overline{\text{IRQ}}$
E	ADDR 4	5	N.C.
F	ADDR 5	6	N.C.
H	ADDR 6	7	RESET
J	ADDR 7	8	DATA 7
K	ADDR 8	9	DATA 6
L	ADDR 9	10	DATA 5
M	ADDR 10	11	DATA 4
N	ADDR 11	12	DATA 3
P	ADDR 12	13	DATA 2
R	ADDR 13	14	DATA 1
S	ADDR 14	15	DATA 0
T	ADDR 15	16	VM HORIZ
U	PHASE 2	17	VM VERT
V	READ/WRITE	18	+8 VOLTS
W	$\overline{\text{READ/WRITE}}$	19	VECTOR FCH
X	+16 VOLTS	20	N.C.
Y	$\overline{\text{PHASE 2}}$	21	N.C.
Z	$\overline{\text{RAM R/W}}$	22	GROUND

WIRE ASSIGNMENTS WITHIN THE 60 PIN RIBBON CABLE

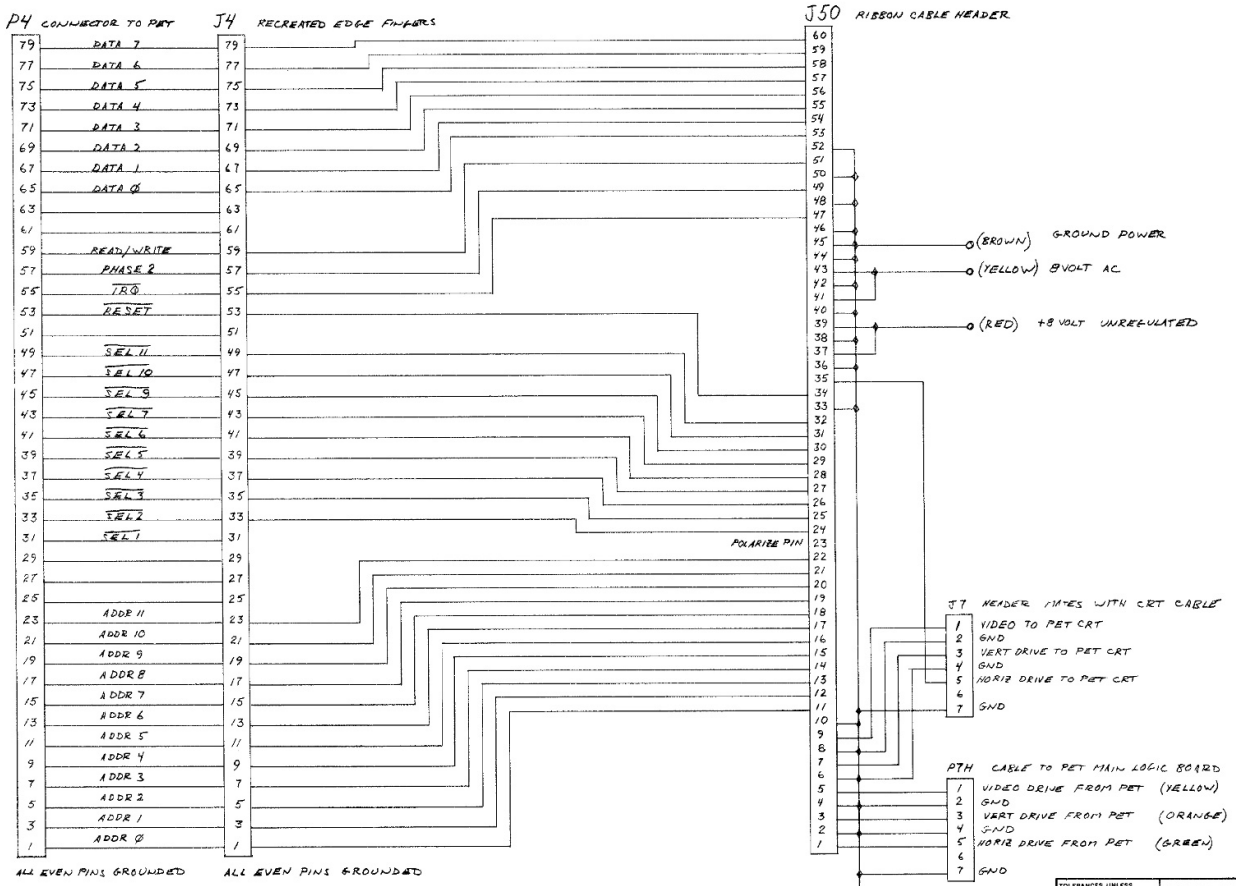
1	HORIZ DRIVE FROM PET	31	SELECT 10
2	GROUND	32	SELECT 11
3	VERT DRIVE FROM PET	33	GROUND
4	GROUND	34	RESET
5	VIDEO DRIVE FROM PET	35	HORIZ DRIVE TO PET MONITOR
6	GROUND	36	GROUND
7	VERT DRIVE TO PET MONITOR	37	+8 VOLTS UNREGULATED
8	GROUND	38	GROUND
9	VIDEO DRIVE TO PET MONITOR	39	+8 VOLTS UNREGULATED
10	GROUND	40	GROUND
11	ADDRESS 0	41	8 VOLTS AC
12	ADDRESS 1	42	GROUND
13	ADDRESS 2	43	8 VOLTS AC
14	ADDRESS 3	44	GROUND
15	ADDRESS 4	45	GROUND
16	ADDRESS 5	46	GROUND
17	ADDRESS 6	47	IRQ
18	ADDRESS 7	48	GROUND
19	ADDRESS 8	49	PHASE 2
20	ADDRESS 9	50	GROUND
21	ADDRESS 10	51	READ/WRITE
22	ADDRESS 11	52	GROUND
23	NO CONNECTION (POLARIZER)	53	DATA 0
24	SELECT 2	54	DATA 1
25	SELECT 3	55	DATA 2
26	SELECT 4	56	DATA 3
27	SELECT 5	57	DATA 4
28	SELECT 6	58	DATA 5
29	SELECT 7	59	DATA 6
30	SELECT 9	60	DATA 7

PIN ASSIGNMENTS IN LIGHT PEN/RESET CONNECTOR

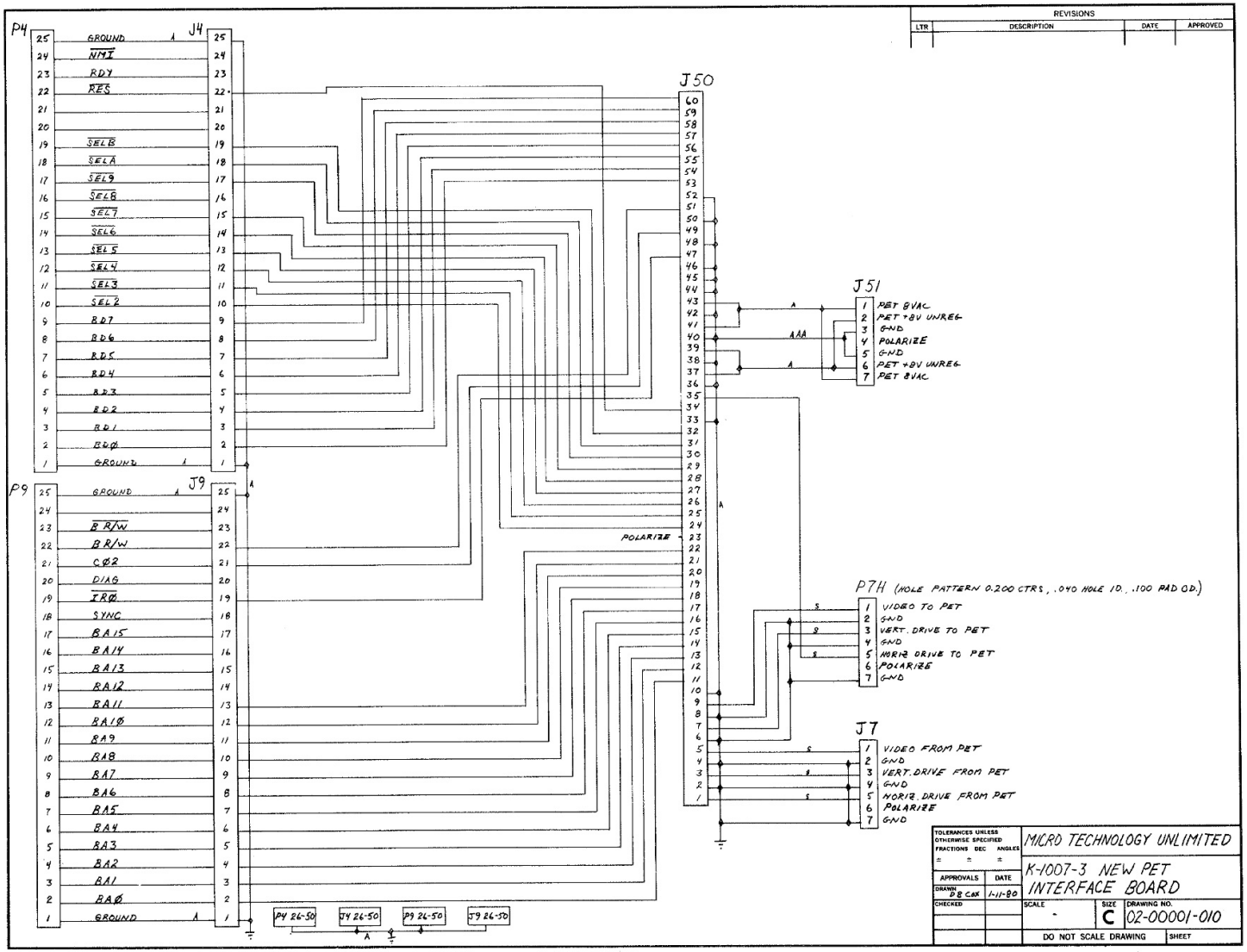
This connector is a 7-pin (two pins cut off for keying purposes) black header at the rear of the board. Pin 1 is marked with a large dot in the printed circuit etch.

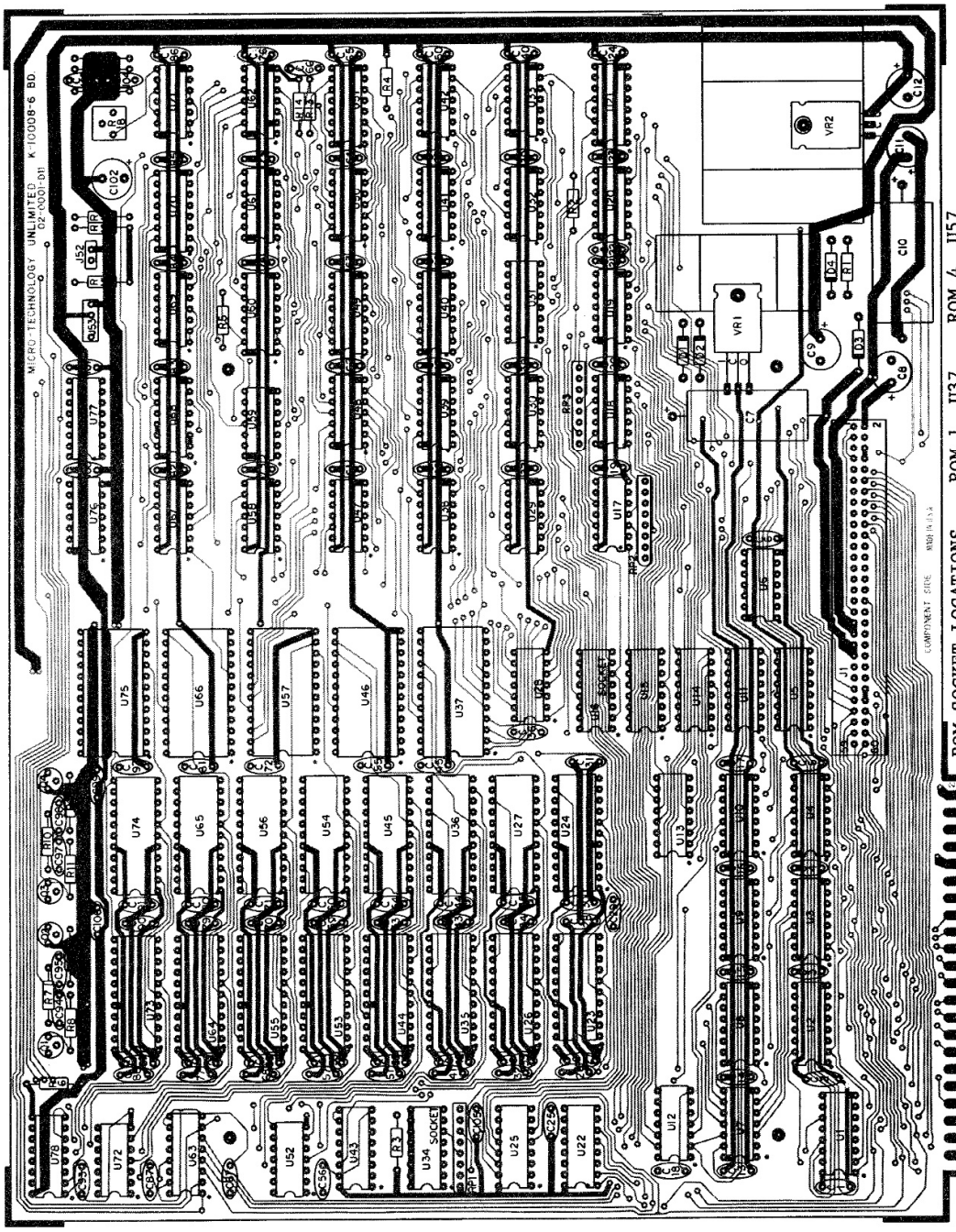
PIN NUMBER	SIGNAL
1	Light pen input
2	Ground
3	(key)
4	+5 volts to light pen (50MA max drain)
5	(key)
6	Reset switch high
7	Reset switch low

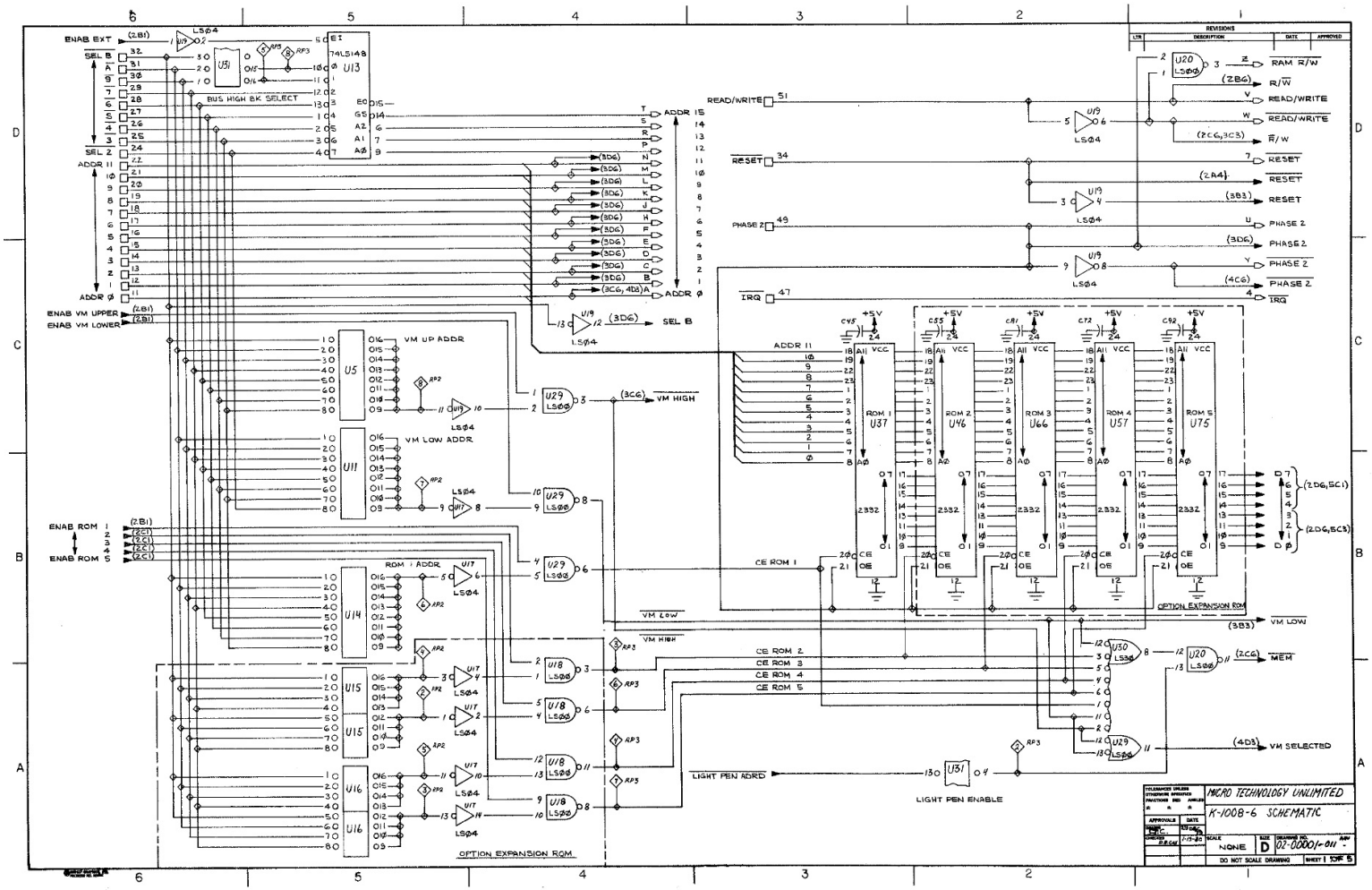
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

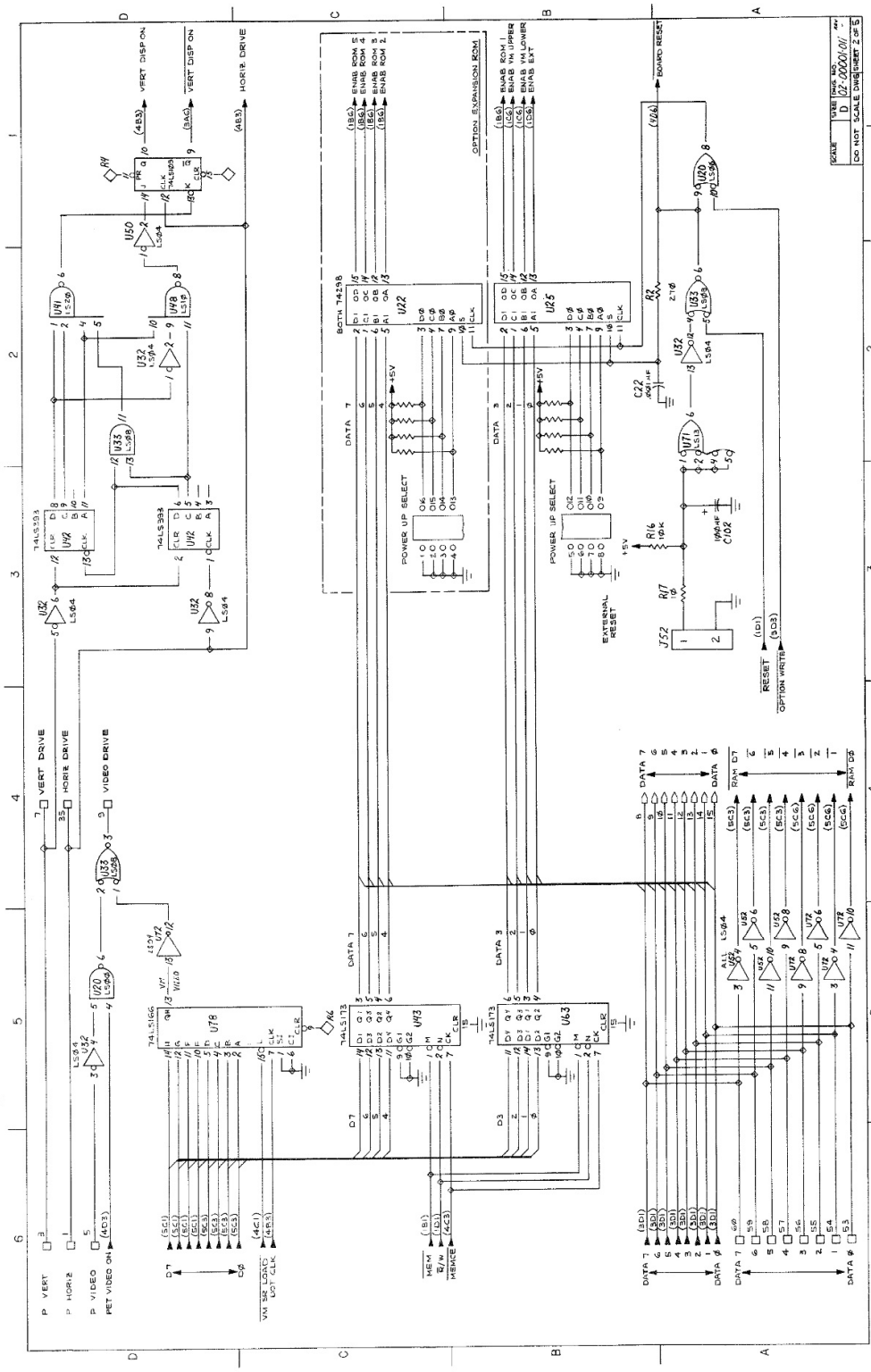


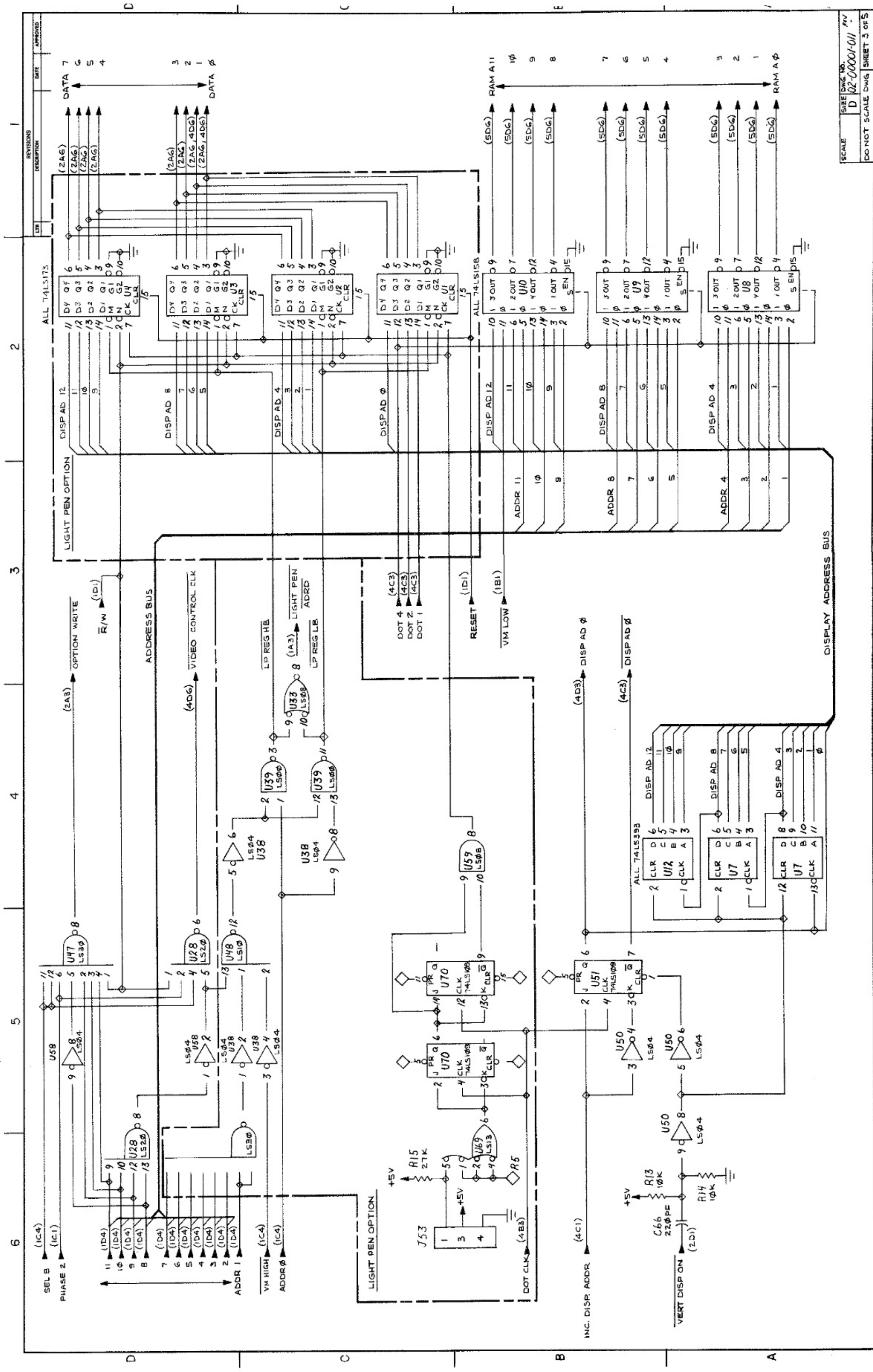
TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±	MICRO TECHNOLOGY UNLIMITED		
APPROVALS	DATE	K-1007-2 CONNECTOR BOARD	
DRAWN DEC,	4-8-80		
CHECKED		SCALE -	SIZE C
		DRAWING NO. 02-00001-009	
		DO NOT SCALE DRAWING	SHEET 1 of 1

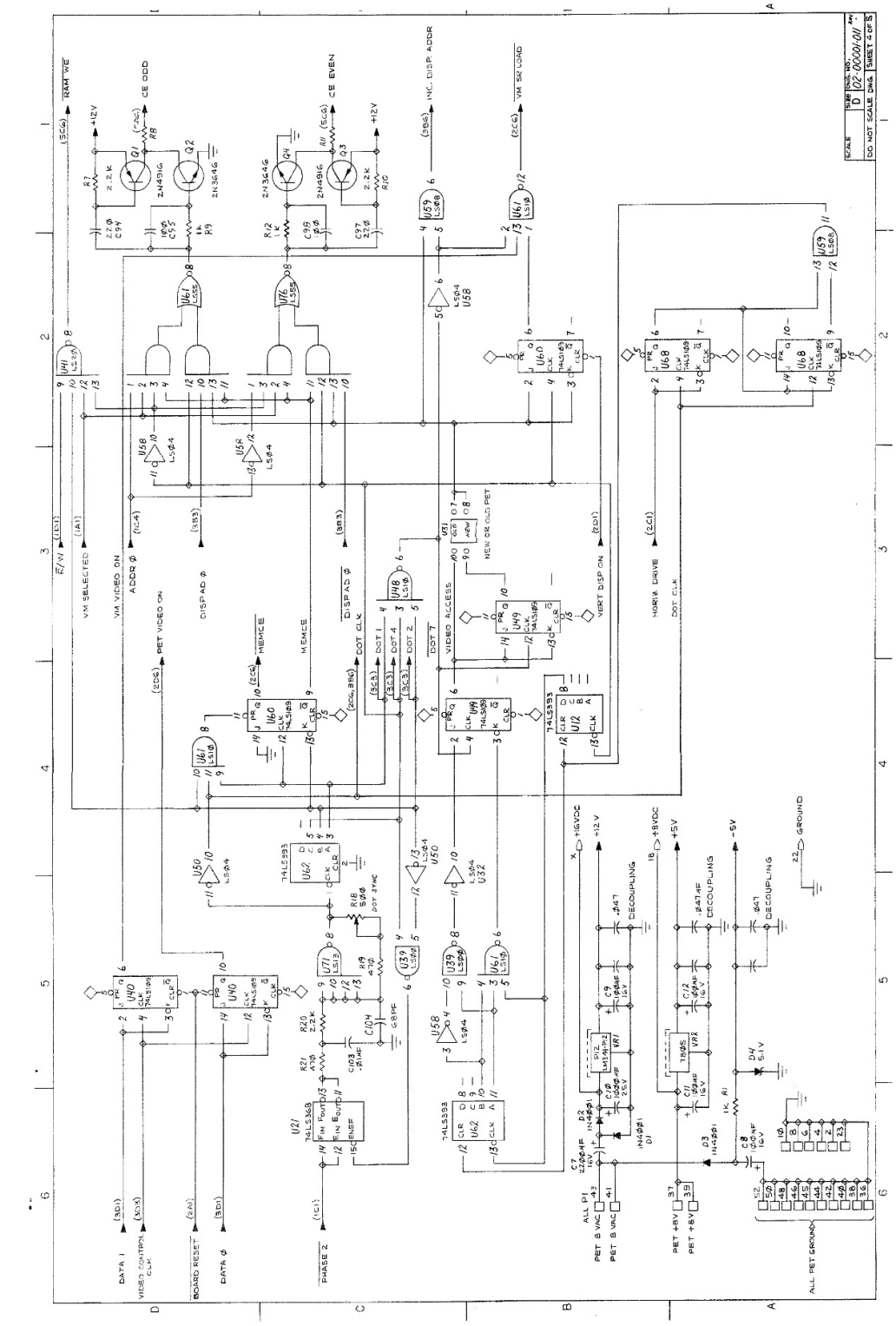

REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
P4
J4
25 GROUND
24 NMI
23 RDY
22 RES
21
20
19 SEL8
18 SEL A
17 SEL9
16 SEL8
15 SEL7
14 SEL6
13 SEL5
12 SEL4
11 SEL3
10 SEL2
9 BD7
8 BD6
7 BD5
6 BD4
5 BD3
4 BD2
3 BD1
2 BDØ
1 GROUND
P9
J9
25 GROUND
24
23 B R/W
22 B R/W
21 CØ2
20 DIAG
19 IRQ
18 SYNC
17 BA15
16 BA14
15 BA13
14 BA12
13 BA11
12 BA1Ø
11 BA9
10 BA8
9 BA7
8 BA6
7 BA5
6 BA4
5 BA3
4 BA2
3 BA1
2 BAØ
1 GROUND
P4 26-50
J4 26-50
P9 26-50
J9 26-50
J50
POLARIZE
J51
1 PET 8VAC
2 PET +8V UNREG
3 GND
4 POLARIZE
5 GND
6 PET +8V UNREG
7 PET 8VAC
P7H (HOLE PATTERN 0.200 CTRS., .040 HOLE I.D., .100 PAD O.D.)
1 VIDEO TO PET
2 GND
3 VERT. DRIVE TO PET
4 GND
5 HORIZ DRIVE TO PET
6 POLARIZE
7 GND
J7
1 VIDEO FROM PET
2 GND
3 VERT. DRIVE FROM PET
4 GND
5 HORIZ. DRIVE FROM PET
6 POLARIZE
7 GND
TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
APPROVALS DATE
DRAWN D B CAN 1-11-80
CHECKED
MICRO TECHNOLOGY UNLIMITED
K-1007-3 NEW PET INTERFACE BOARD
SCALE -
SIZE C
DRAWING NO. 02-00001-010
DO NOT SCALE DRAWING
SHEET

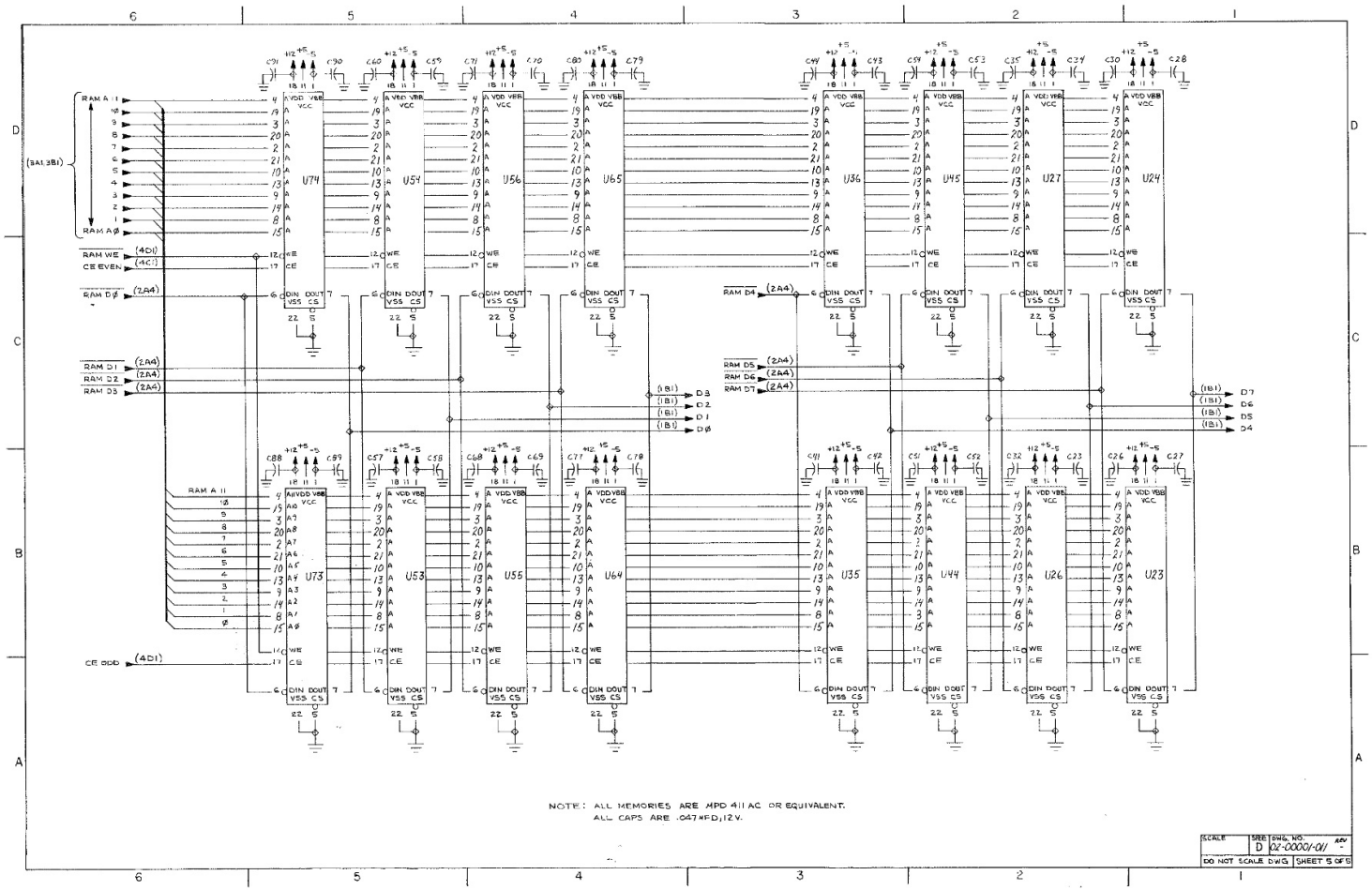

MICRO-TECHNOLOGY UNLIMITED K-100008-6 BD
02-0001-01
ROM SOCKET LOCATIONS
ROM 1 U37
ROM 2 U46
ROM 3 U66
ROM 4 U57
ROM 5 U75


ENAB EXT
SEL B
SEL A
SEL Z
ADDR 11
ADDR Ø
ENAB VM UPPER
ENAB VM LOWER
ENAB ROM 1
ENAB ROM 5
BUS HIGH BK SELECT
74LS148
ADDR 15
ADDR Ø
SEL B
VM UP ADDR
VM LOW ADDR
VM HIGH
VM LOW
ROM 1 ADDR
OPTION EXPANSION ROM
READ/WRITE
RESET
PHASE 2
IRQ
RAM R/W
R/W
PHASE 2
CE ROM 1
CE ROM 2
CE ROM 3
CE ROM 4
CE ROM 5
MEM
VM SELECTED
LIGHT PEN ADRD
LIGHT PEN ENABLE
ROM 1 U37
ROM 2 U46
ROM 3 U66
ROM 4 U57
ROM 5 U75
REVISIONS
MICRO TECHNOLOGY UNLIMITED
K-1008-6 SCHEMATIC
NONE
02-00001-011
DO NOT SCALE DRAWING




LIGHT PEN OPTION
ALL 74LS173
ALL 74LS158
ALL 74LS393
DISPLAY ADDRESS BUS
ADDRESS BUS
VIDEO CONTROL CLK
OPTION WRITE
RESET
VM LOW
DOT CLK
INC. DISP. ADDR
VERT DISP ON
SEL B
PHASE 2
DATA 7
DATA Ø
RAM A11
RAM A Ø
DO NOT SCALE DWG
SHEET 3 OF 5





NOTE: ALL MEMORIES ARE MPD 411 AC OR EQUIVALENT.
ALL CAPS ARE .047 MFD, 12V.

SCALE	SIZE	DWG. NO.	REV
	D	02-0000-01	-
DO NOT SCALE DWG		SHEET 5 OF 6	